YOR920000174
09/612,260

REMARKS

Claims 1-20 and 44-51 are all the claims pending in the application. Claims 21-43 are cancelled, above, pursuant to a previous restriction requirement. Claims 44-51 are added, above, to further define the invention. Claims 1-20 stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1, 4, 7, 8 and 10 stand rejected under 35 U.S.C. §102(e) as being anticipated by Kumagai (US Patent No. 6,188,111). Claims 2-3 and 9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kumagai. Claims 6, 11, 14, 16 and 18-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kumagai in view of Pfiester (US Patent No. 5,166,084). Claims 5 and 17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kumagai in view of Uesugi et al. (US Patent No. 5,708,286) hereinafter referred to as Uesugi. Applicants respectfully traverse these rejections based on the following discussion.

A. The 35 U.S.C. §§102 and 103 Rejections Based on Kumagai

The structure defined by independent claims 1 and 11 is shown, for example, in Applicants' Figure 47. This figure illustrates the first gate 16 on top of the channel region 5, and the second gate 22 below the channel region 5. With the invention, the first gate and the second gate are electrically separated from each other. An important feature of the claimed invention is that the first and second gates are "self-aligned" with each other (as defined by independent claims 1 and 11). More specifically, the sacrificial nitrides 2 and 7 which are eventually replaced by the conductive upper and lower gates 16, 22 are defined in the self-aligned processing shown

in Figure 7. This self-alignment defines a structure where the upper and lower gates will be consistently formed in an aligned manner.

To the contrary, the applied reference Kumagai includes an upper gate 145 that is formed during a separate processing cycle than the lower gate 140. Therefore, the structure shown and Kumagai will not consistently place the upper gate 145 in alignment with the lower gate 140. Such mis-aligned structures add parasitic capacitance to the device, which reduces the device's performance. To the contrary, since the claims define that the first and second gates are "self-aligned", the claimed structure consistently includes the upper gate and lower gate being aligned with one another.

Therefore, since Kumagai does not teach or suggest a structure where the upper gate 145 is "self-aligned" with the lower gate 140, it cannot teach or suggest the structure defined by independent claims 1 and 11. Therefore, independent claims 1 and 11 are patentable over Kumagai. Further, dependent claims 2-4 and 7-10 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view the forgoing, the Examiner is respectfully requested to reconsider and withdraw these rejections.

B. The Rejection Based on Kumagai in view of Pfiester

As shown above, Kumagai does not teach or suggest the invention as defined by independent claims 1 or 11 because Kumagai fails to teach a number of features defined by independent claims 1 and 11, including the upper and lower gates being "self-aligned." The Office Action makes reference to Pfiester for allegedly teaching that the first gate electrodes can comprise a different material than the second gate electrodes. However, Pfiester actually forms the lower gate 24 by doping a portion of the substrate 12. Therefore, Pfiester cannot teach or suggest upper and lower gates that are "self-aligned" with each other. The actual alignment of the lower gate 24 is imprecise because this gate is formed in an implantation process. The

amount by which the impurity spreads within the substrate 12 within Pfiester is highly uncontrolled. Therefore, the size of the gate will not be truly "self-aligned" within the meaning of the claimed invention, because the claimed structure produces a tightly controlled size of each of the gates. Further, Pfiester does not teach or suggest that the first gate "comprises a different material than said second gate" as defined by independent claim 11. To the contrary, the lower gate 24 in Pfiester is merely a doped region of the substrate and is not truly a separate gate material. Thus, the doped region 24 within Pfiester would not teach or suggest to one ordinarily skilled in the art the second gate that is defined by independent claims 11. The doping concentrations that are used to change the conductivity of a silicon substrate are extremely small on the molecular level (only a few percent) and do not actually create a separate material. Therefore, Pfiester does not actually teach a separate lower gate, but instead merely teaches a region within the substrate which is has slightly different chemical properties from the surrounding substrate. Thus, there will not be any structural "self-aligned" upper and lower gates as defined by independent claims 1 and 11, if one ordinarily skilled in the art were to make a structure according to the teaching within Pfiester and/or Kumagai.

Therefore, Applicants submit that even if one ordinarily skilled in the art had combined Kumagai and Pfiester, as proposed in the Office Action, the combination would not teach or suggest the invention as defined by independent claims 1 and 11. Thus, independent claims 1 and 11 are patentable over the proposed combination. Further, dependent claims 6, 14, 16, and 18-20 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the forgoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

C. The Rejection Based on Kumagai in view of Uesugi

As shown above, Kumagai does not teach or suggest the invention as defined by independent claims 1 or 11 because Kumagai fails to teach a number of features defined by independent claims 1 and 11, including the upper and lower gates being "self-aligned." Uesugi is referenced for the limited purpose of allegedly showing coplanar contacts. However, Uesugi does not teach or suggest upper and lower gates that are aligned (much last self-aligned). To the contrary, the upper gate 60 and lower gate 30 shown in Figure 41 of Uesugi actually affect different channel regions (ch1, ch2) and are not truly upper and lower gates that border a channel region. Further, as illustrated by Figure 41 of Uesugi, the gates 30, 60 are not aligned.

Therefore, Applicants respectfully submit that if one ordinarily skilled in the art had combined Kumagai and Uesugi as suggested in the Office Action, any such combination would not teach or suggest a structure having "self-aligned" upper and lower gates, as defined by independent claims 1 and 11. Therefore, independent claims 1 and 11 are patentable over the combination of Kumagai and Uesugi suggested in the Office Action. Further, dependent claims 5 and 17 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view the forgoing, the Examiner is respectfully requested to reconsider and withdraw this rejection

II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-20, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

YOR920000174
09/612,260

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 50-0510.

Respectfully submitted,

Dated: 7/18/02

Frederick W. Gibb, III
Reg. No. 37,629

McGinn & Gibb, P.C.
2568-A Riva Road
Suite 304
Annapolis, MD 21401
Customer Number: 28211

YOR920000174
09/612,260

Marked Up Version of Changes Made:

1. (Amended) A transistor comprising:
a channel region;
a first gate on top of said channel region;
a second gate below said channel region; and
an isolation layer below said second gate,
wherein said first gate and said second gate are self-aligned and electrically separated from each other.

11. (Amended) A semiconductor chip having at least one transistor, said transistor comprising:
a channel region;
a first gate on top of said channel region;
a second gate below said channel region; and
an isolation layer below said second gate,
wherein said first gate is self-aligned with and comprises a different material than said second gate.

Please cancel claims 21-43.

Please add the following new claims:

44. A transistor comprising:
a channel region;
a first gate on top of said channel region;

a second gate below said channel region;

an isolation layer below said second gate; and

source and drain regions laterally adjacent said channel region,

wherein said source and drain regions are self-aligned with said first gate and said second gate, such that said source and drain regions do not horizontally overlap said first gate or said second gate, and

wherein said first gate and said second gate are electrically separated from each other.

45. A transistor comprising:

a channel region;

a first gate on top of said channel region;

a second gate below said channel region;

an isolation layer below said second gate; and

source and drain regions laterally adjacent said channel region, said first gate, and said second gate,

wherein said first gate and said second gate are electrically separated from each other.

46. The transistor in claim 1, wherein said self-aligned nature of said first gate and said second gate positions said first gate above and aligned with said second gate.

47. The transistor in claim 4, further comprising:

source and drain regions laterally adjacent said channel region, said first gate, and said second gate; and

source and drain dielectrics between said source and drain regions and said first gate and said second gate,

wherein a thickness and material selection of said first gate dielectric and said second gate dielectric is independent of said source and drain dielectrics.

YOR920000174
09/612,260

48. The semiconductor chip in claim 11, further comprising source and drain regions laterally adjacent said channel region, wherein said source and drain regions are self-aligned with said first gate and said second gate, such that said source and drain regions do not horizontally overlap said first gate or said second gate.

49. The semiconductor chip in claim 11, wherein said self-aligned nature of said first gate and said second gate positions said first gate above and aligned with said second gate.

50. The semiconductor chip in claim 11, further comprising source and drain regions laterally adjacent said channel region, said first gate, and said second gate.

51. The semiconductor chip in claim 14, further comprising:

source and drain regions laterally adjacent said channel region, said first gate, and said second gate; and

source and drain dielectrics between said source and drain regions and said first gate and said second gate,

wherein a thickness and material selection of said first gate dielectric and said second gate dielectric is independent of said source and drain dielectrics.